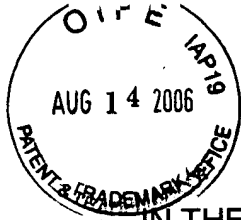


X-1292 US
10/796,750



PATENT
Conf. No.: 2526

IN THE UNITED STATES PATENT OFFICE

Applicants: Vasisht Mantra Vadi, et al.
Assignee: Xilinx, Inc.
Title: "Segmented Dataline Scheme in a Memory with Enhanced Full Fault Coverage Memory Cell Testability"
Serial No.: 10/796,750 File Date: March 8, 2004
Examiner: Trong Q. Phan Art Unit: 2827
Docket No.: X-1292 US Conf. No.: 2526

Mail Stop RCE
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT FILED WITH AN RCE

Dear Sir:

Please amend the above-identified application as indicated beginning on the following page.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 11 of this paper.